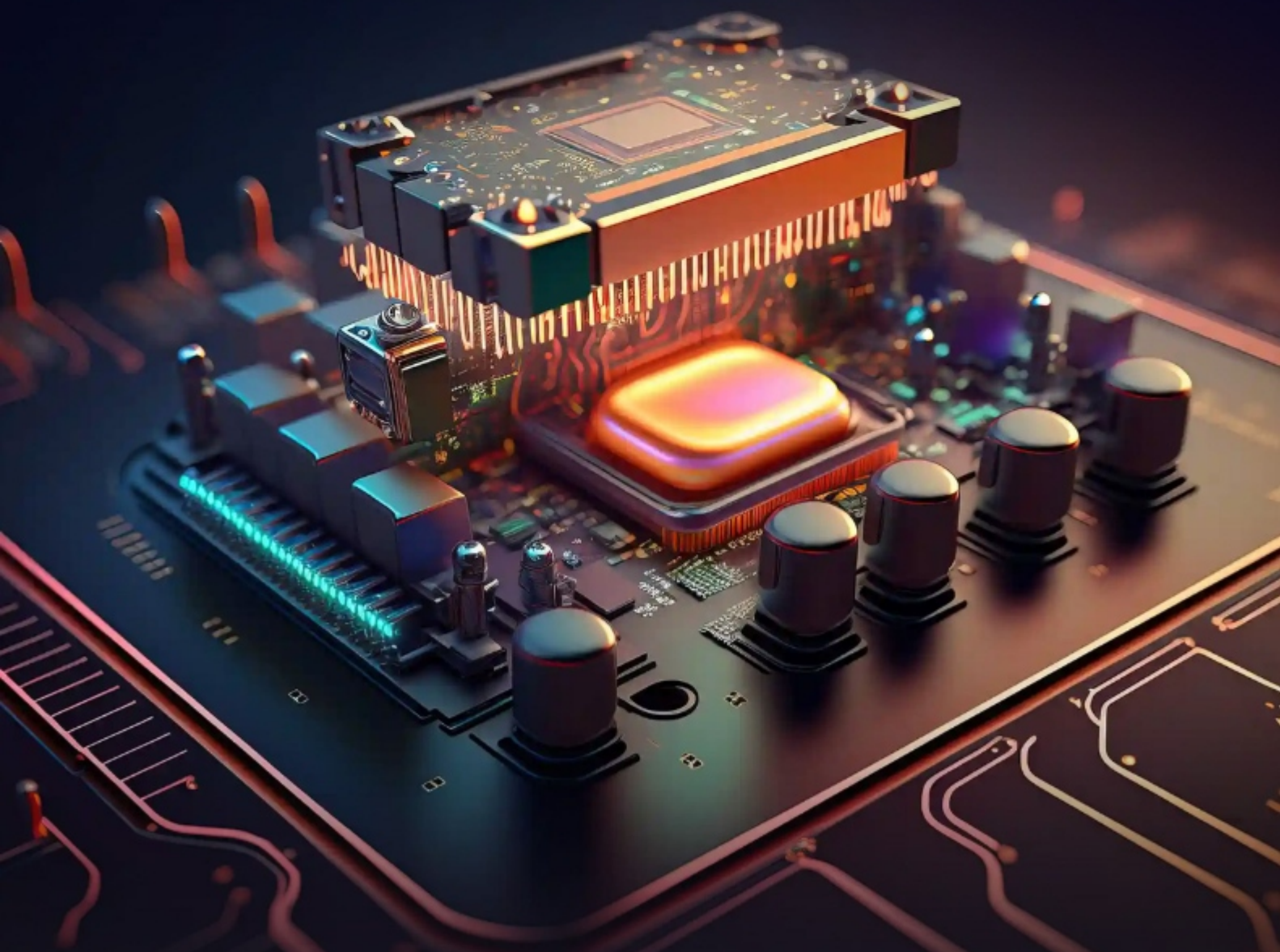
भारतीय प्रौद्योगिकी संस्थान दिल्ली
Indian Institute of Technology Delhi

Harness the **Power of VLSI** *Design Innovation*

CERTIFICATE PROGRAMME IN
DIGITAL VLSI DESIGN

Programme by **CEP, IIT Delhi**



Programme offered by Continuing Education Programme (CEP), IIT Delhi

DRIVE TANGIBLE GROWTH IN THE BLOOMING SEMICONDUCTOR INDUSTRY

INDUSTRY GROWTH

The Semiconductors market in the world is projected to grow **by 6.30%** (2024-2027) resulting in a market volume of **US$736.40 billion in 2027.**

*Statistia

India's semiconductor **market** to touch **$64 billion by 2026.**

*Business Standard

Recognising the need to reduce its dependence on imported semiconductors **MeitY** has unveiled a **$10 billion commitment** towards the **India Semiconductor Mission.**

*Inc42

JOB MARKET

At the second Semicon India Future Design roadshow held in Bengaluru IISc campus, **Union Minister** Rajeev Chandrasekhar said that India plans to produce a minimum of **85,000** global semiconductor **talent** in the next **two years.**

*Analytics India Mag

The workforce for the **semiconductor** industry will need to **increase** by more than **1 million** skilled people by **2030 as per Deloitte.** Over **1 lakh engineering** and smart manufacturing graduates will be required for this industry. Generative AI will transform all industries, entire workforce in years to come and add over **$7 trillion** to the global economy). This AI wave is solely hinged on the capacity to develop and design Semiconductors.

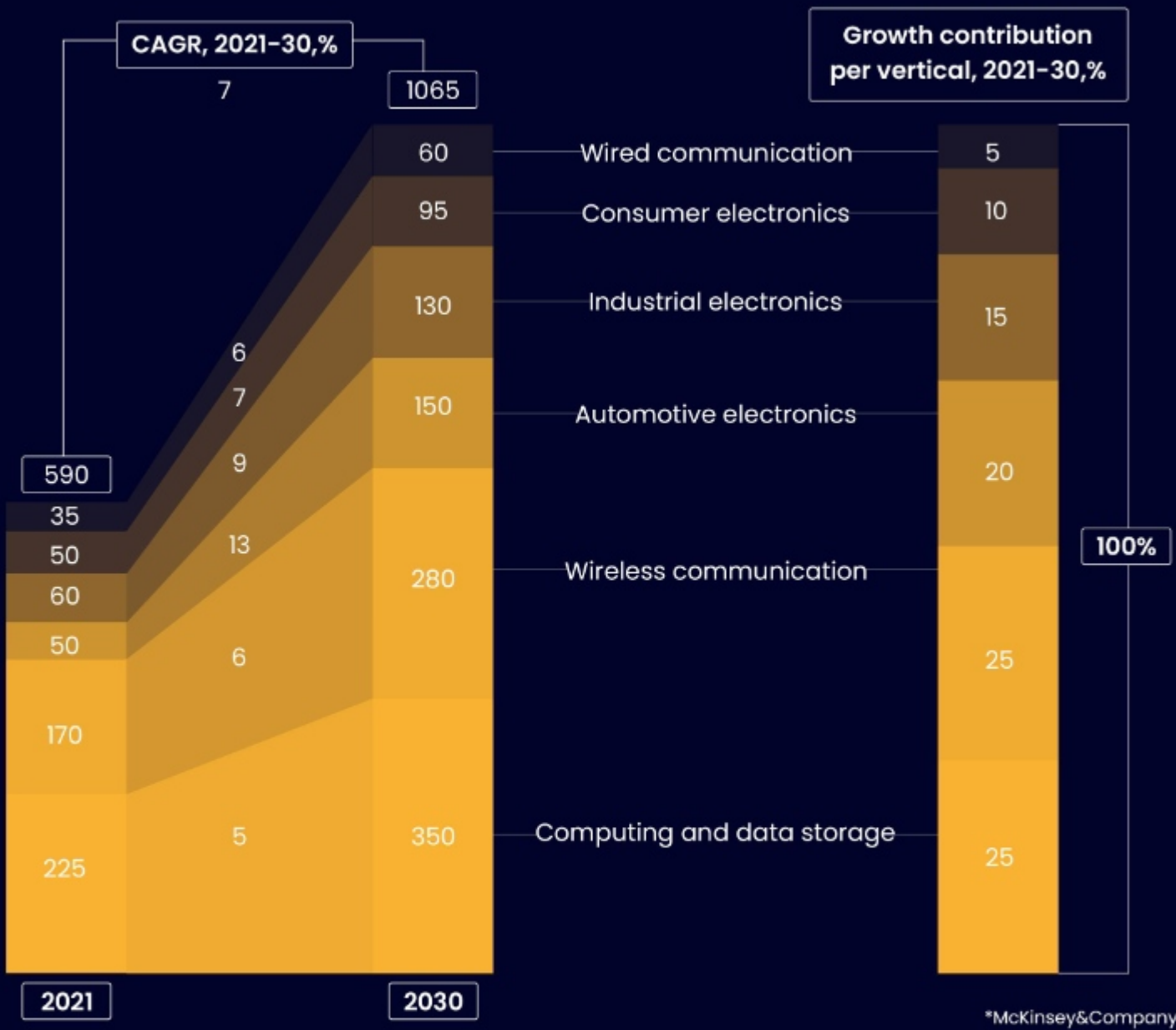
*Financial Express

India is becoming a great conductor for the semiconductor industry, Prime Minister Narendra Modi said on July 28, adding that the government has identified more than 300 colleges where semiconductor courses will be available and India will have more than 1 lakh semicon design engineers in the next five years. Though the industry is still at a nascent stage, there are currently around 8,000 open positions in the semiconductor sector across job profiles and levels, according to the data put together for Moneycontrol by TeamLease EdTech.

*Moneycontrol

THE GLOBAL SEMICONDUCTOR MARKET'S METEORIC RISE FUELED BY AUTOMOTIVE, DATA STORAGE, WIRELESS

Global semiconductor market value by vertical, indicative, $billion

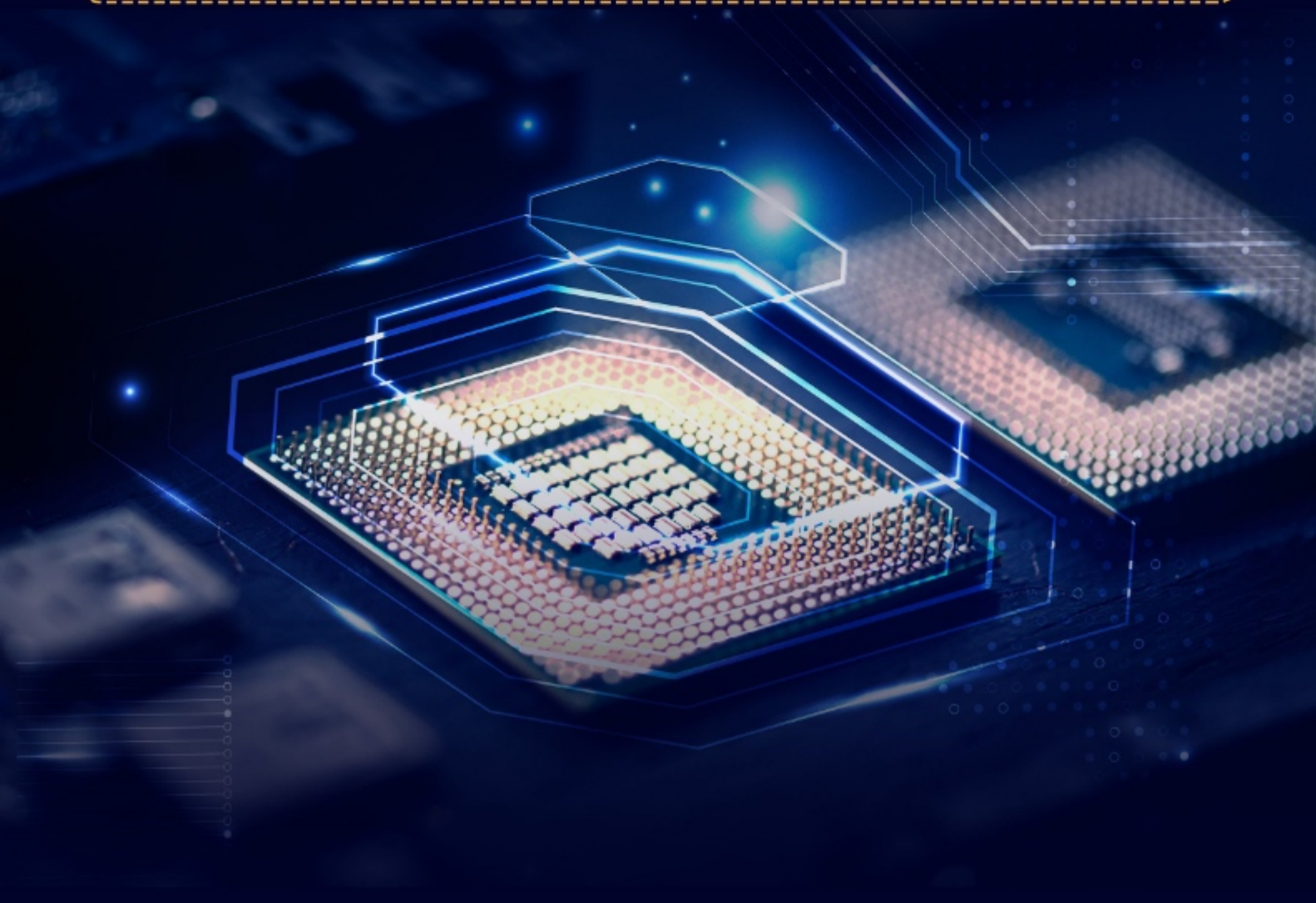


*McKinsey&Company

Shedding light on digital VLSI chip design, the locomotive propels the AI train forward. As artificial intelligence permeates industries, robust chip design becomes imperative. VLSI chip innovation accelerates computational prowess and energy efficiency by driving tangible growth in the blooming semiconductor industry. With cutting-edge architectures and design methodologies, engineers sculpt silicon marvels, empowering AI applications from edge to cloud. This relentless pursuit of efficiency and performance fuels technological advancement and underpins economic growth. Through meticulous design iterations and collaborative research, digital VLSI chip design pioneers the next era of computing, shaping a smarter, interconnected world.

OVERVIEW

As the global semiconductor industry hurtles towards a projected trillion-dollar valuation by 2030, the demand for specialized Digital Integrated Circuits surges. To address the need, stay ahead of the curve by pursuing a comprehensive Certification Programme in Digital VLSI Design, facilitated by esteemed faculty from the Centre for Applied Research in Electronics (CARE) at IIT Delhi, prepares participants to navigate this burgeoning landscape with confidence and expertise. Covering essential aspects such as RTL design, synthesis, verification, and testing, the programme equips participants with practical skills and theoretical knowledge. Through hands-on exposure to industry-standard tools and methodologies, including CAD tools, hardware description languages (HDLs), and simulation tools, participants are primed for success in semiconductor companies, electronics design firms, or research institutions. Moreover, our emphasis on immersive projects and case studies fosters participants' problem-solving capabilities, empowering them to tackle intricate design challenges with efficacy. Join this interdisciplinary programme to transform into a proficient and sought-after professional in the dynamic realm of Digital VLSI Design.



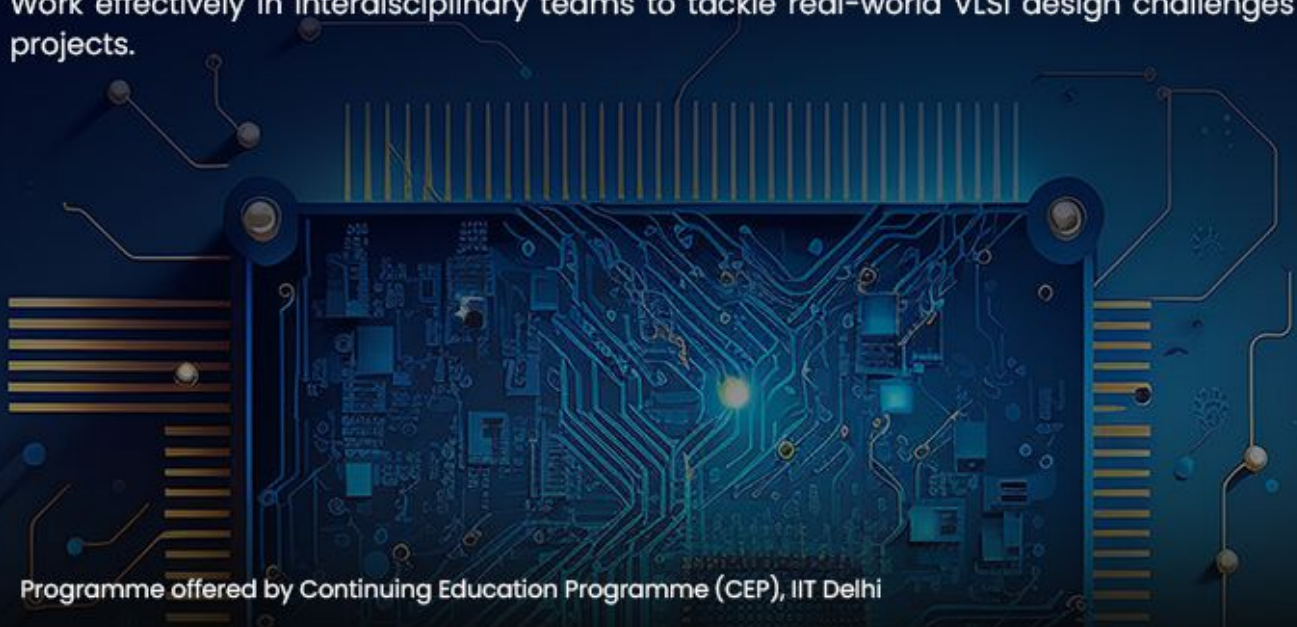
PROGRAMME HIGHLIGHTS

- Certification from CEP, IIT Delhi
- Learn from top faculty in VLSI Design
- 3 Days Campus Immersion
- Real-world Case Studies
- Industries Visits/Interactions with the Leaders
- Networking Opportunities during Campus Immersion

LEARNING OUTCOMES

Upon successful completion of this programme, participants should be able to:

- Demonstrate a solid understanding of design principles, including logic synthesis, timing analysis, and physical design.
- Utilize industry-standard VLSI design softwares to design, simulate, and verify digital integrated circuits.
- Apply advanced VLSI design techniques such as low-power design, high-speed design, and design for testability (DFT).
- Analyze and optimize the performance, area, and power consumption of digital VLSI designs.
- Work effectively in interdisciplinary teams to tackle real-world VLSI design challenges and projects.



Programme offered by Continuing Education Programme (CEP), IIT Delhi

PROGRAMME CONTENT

MODULE-1: DIGITAL IC DESIGN

- CMOS ASIC Design Flow
- CMOS Circuit Design
- Delay, Setup and Hold Time Analysis
- Combinational and Sequential Circuits
- High Performance Design
- Low-Power Design

This module provides a fundamental understanding of the principles and techniques involved in designing complex integrated circuits. This includes learning about logic gates, flip-flops, sequential circuits, and other essential building blocks of digital systems. This module intersects with various disciplines, including computer science, electrical engineering, and physics. Students from diverse backgrounds can benefit from learning digital IC design principles and apply them to interdisciplinary projects and collaborations.

MODULE-2: DIGITAL CIRCUIT AND RTL DESIGN

- CMOS Standard Cells, GPIOs
- Custom blocks e.g. Level-shifters
- Power Management (PMIC) Blocks
- RTL implementation and Verification
- Design Synthesis
- DFT, Scan and ATPG

Digital circuits and RTL design is fundamental for anyone interested in designing electronic systems, ranging from simple logic gates to complex microprocessors and system-on-chip (SoC) designs. This typically involves hands-on projects using industry-standard design tools such as Verilog or VHDL. This practical experience is invaluable for developing proficiency in using these tools, which are widely used in the industry. These skills are highly sought after in the semiconductor industry, as well as in fields such as embedded systems, FPGA (Field-Programmable Gate Array) design, and ASIC (Application-Specific Integrated Circuit) design. Completing a course in this area prepares students for roles such as digital design engineer, verification engineer, and FPGA designer.

MODULE-3: PHYSICAL DESIGN

- Floor-Plan
- Placement
- Static Timing Analysis
- Clock Tree Synthesis and Signal Integrity
- Routing and DRC
- Layout Parasitic Extraction

Physical design provides insights into the manufacturing process of integrated circuits, including semiconductor fabrication techniques, layout design rules, and manufacturing constraints. Candidates gain an appreciation for the intricacies involved in translating circuit designs into physical layouts that can be fabricated into silicon chips. It involves hands-on projects using industry-standard Electronic Design Automation (EDA) tools such as Cadence Virtuoso, Synopsys ICC, or Mentor Graphics Calibre. Students acquire practical experience in layout design, floor planning, placement, routing, and physical verification, which are essential skills for IC design engineers.

PROGRAMME CONTENT

MODULE-4: SUPPLEMENTARY TOPICS

- Unix Environment
- Shell/Tcl/Perl/Python Scripting
- Verilog Model Development
- Post Silicon Chip Validation
- Chip Integration and Packaging
- Interview FAQs

These topics for chip design provide additional depth and breadth to candidates' understanding of integrated circuit (IC) design and semiconductor technology. These topics cover advanced design methodologies and techniques beyond the basics taught in core courses. By including these supplementary topics in a chip design curriculum, instructors will provide candidates with a well-rounded education that prepares them for the diverse challenges and opportunities in the rapidly evolving field of integrated circuit design and semiconductor technology.

LAB MODULE

- 24 hours of Lab module is planned in the programme.
- Labs will be conducted online. Various projects and hands-on training will be provided during lab hours.

TOOLS

01 **Circuit Simulation Tool:** LTSpice

02 **Verilog Simulation Tool:** ModelSim

03 **FPGA/RTL Design Tool:** Xilinx Vivaldo

04 **FPGA Development Tool:** Quartus Prime Lite

05 **Operating System and Languages:** Linux/Tcl

PROJECTS

Some of the projects planned are given below:

Project 1: Combinational and Sequential CMOS Circuit Design

In this project, designing CMOS circuits, whether combinational or sequential, involves considerations such as power consumption, speed, area utilization, and noise immunity. CMOS technology offers advantages such as low power consumption, high noise immunity, and scalability, making it suitable for a wide range of digital applications from simple logic gates to complex microprocessors and system-on-chip (SoC) designs.

PROGRAMME CONTENT

Understanding both combinational and sequential circuit design principles is essential for building efficient and reliable digital systems.

Project 2: CMOS Low Power I/O Circuit Design

Designing CMOS low-power I/O circuits requires a careful balance between power efficiency, performance, and reliability. In this project, by leveraging voltage scaling, transistor sizing, energy-efficient signaling techniques, and other design considerations, candidates can create I/O interfaces that meet stringent power requirements without sacrificing functionality or performance.

Project 3: Power Management IC (PMIC) Design

Power Management IC Design involves the integration of voltage regulators, DC-DC converters, battery management, power sequencing, and monitoring functions into a single integrated circuit to efficiently manage power in electronic systems, optimize energy efficiency, and extend battery life. In this project, candidate will address the key design considerations and by leveraging advanced design techniques, will develop highly efficient and reliable power management solutions for a wide range of applications.

Project 4: Clock Tree Synthesis and Static Timing Analysis

Clock Tree Synthesis (CTS) and Static Timing Analysis (STA) are crucial steps in the design and verification of digital integrated circuits, particularly in high-performance designs where timing constraints are critical. By optimizing the clock distribution network and analysing timing paths, candidates can achieve high-performance and reliable digital designs that operate correctly within specified timing constraints.

Project 5: Design for Test (DFT) and Automatic Test Pattern Generation (ATPG)

Design for Test (DFT) and Automatic Test Pattern Generation (ATPG) are integral parts of the IC design and manufacturing process, aimed at enhancing testability, improving fault detection, and ensuring the quality and reliability of integrated circuits. In this project, by incorporating DFT techniques into the design and employing ATPG tools during test generation, candidates can streamline the testing process and achieve high-quality, reliable electronic systems.

Note: This is an indicative list of course topics and is subject to change as per IIT Delhi's discretion.

PROGRAMME DETAILS

Duration	6-8 Months | 72 Hours of Learning
Delivery	Live Online Sessions delivered through Direct-to-Device (D2D)

SCHEDULE

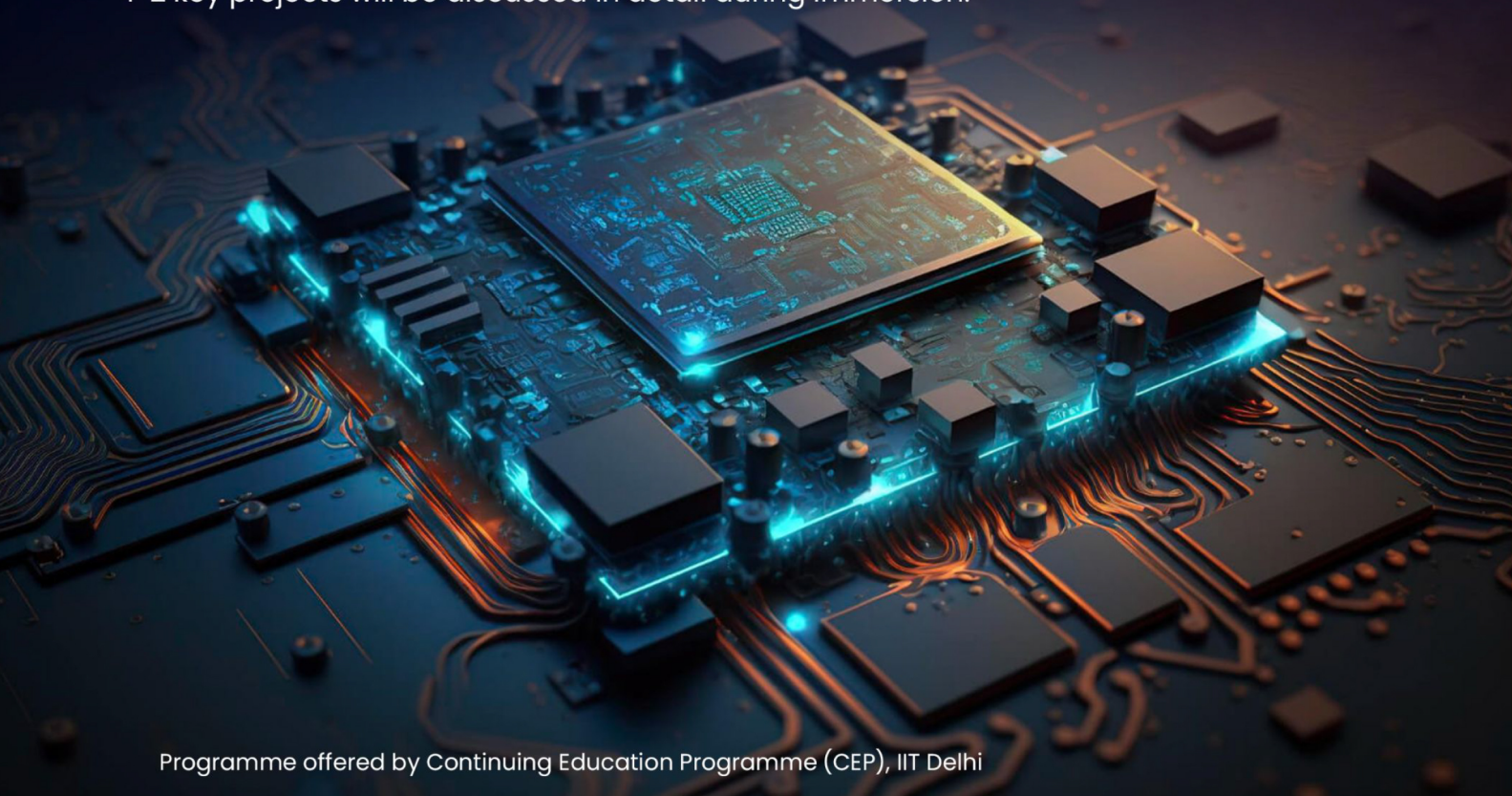
Session Timings: Sunday from 10:00 AM to 1:00 PM

No. of sessions: 4 lecture Modules + 1 Lab Module + 1 Campus Visit

Application Closure Date	1st October 2024
Commencement Date	6th October 2024

CAMPUS IMMERSION

- Campus immersion for a minimum of 3 days based on the willingness of the participants. The cost of travel and stay will be borne by the participants.
- Interaction workshop with industry leaders and experts. Hands-on training on industry standard tools and technology.
- 1-2 key projects will be discussed in detail during immersion.



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PROGRAMME DETAILS

ELIGIBILITY CRITERIA

- Any Electronics, Electrical, Physics or Computer Science Graduate.
- Candidates pursuing the graduation degree are also eligible however preference will be given to applicants with experience.
- Diploma holders (10 + 3) or (10 + 2 + 3) are also eligible.

SCREENING & SELECTION

- Screening and selection will be done by IIT Delhi.

ADMISSION CRITERIA

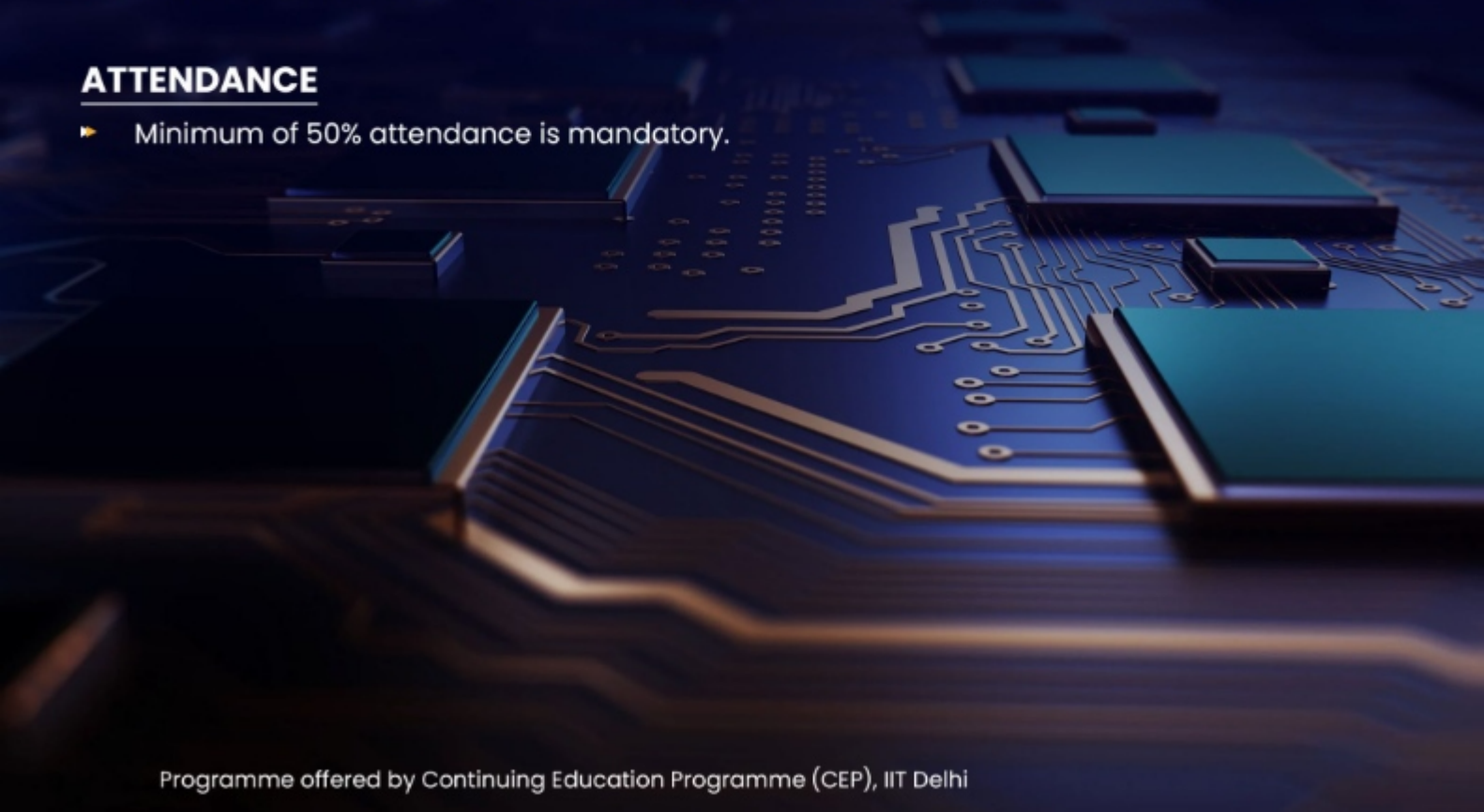
- Admission will be on the basis of academic background, professional background (Work experience) and performance in the interview process. The Programme Coordinator(s) will shortlist the candidates' profiles

ASSESSMENT

- 60% - End of programme MCQ-based exam
- 40% - Assignments & project
- 10% - Attendance (Grace)
- Candidates need to secure a minimum of 50% overall to be eligible for the certificate.

ATTENDANCE

- Minimum of 50% attendance is mandatory.



PROGRAMME FEE DETAILS

Total Programme Fee: INR 1,20,000/- + GST

INSTALMENT PATTERN

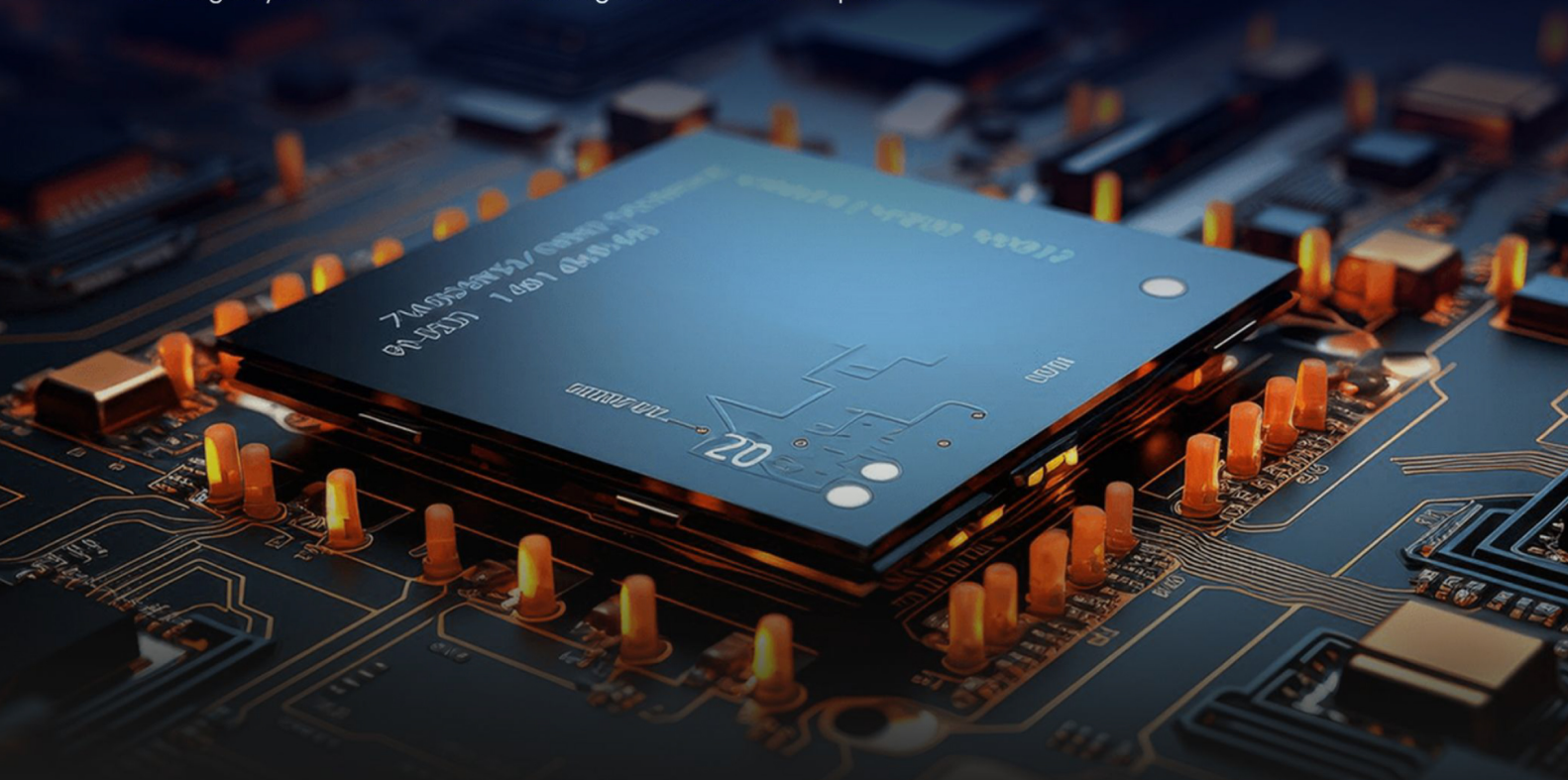
INSTALMENT 1	INR 80,000/- + GST (3 days from date of offer)	INSTALMENT 2	INR 40,000/- + GST (4th October 2024)

EASY EMI OPTIONS AVAILABLE*

- *Payment of fees should be submitted in the IIT Delhi CEP account only and the receipt will be issued by the IIT Delhi CEP account for your records.
- *Loan Options is a service offered by Jaro Education. IIT Delhi is not responsible for the same.

WITHDRAWAL & REFUND FROM PROGRAMME:

- Candidates can withdraw within 15 days from the programme start date. A total of 80% of the total fee received will be refunded. However, the applicable tax amount paid will not be refunded on the paid amount.
- Candidates withdrawing after 15 days from the start of the programme session will not be eligible for any refund.
- If you wish to withdraw from the programme, you must email cepaccounts@admin.iitd.ac.in and crm.supportiitd@jaro.in, stating your intent to withdraw. The refund, if applicable, will be processed within 30 working days from the date of receiving the withdrawal request.



Programme offered by Continuing Education Programme (CEP), IIT Delhi

PROGRAMME CERTIFICATION

Programme Code: .....

Indian Institute of Technology Delhi

HAUZ KHAS, NEW DELHI- 110016

Department/Centre/School of .....

Continuing Education Programme

On

Title of the Programme

This is to certify that

Mr./Ms. **Name Of The Participant**

has successfully completed the online certificate programme on **"Title of the Programme"** held from ..... to ..... by the Indian Institute of Technology Delhi.

Prof.
Programme Coordinator

Prof.
Head of the Department

Prof.
Head/Associate Head, QIP/CEP

An initiative under eVIDYA@IITD (ई-विद्या@IITD)

Candidates who score at least 50% marks overall and have a minimum attendance of 50% will receive a **'Certificate of Completion'** from CEP, IIT Delhi.

Programme Code: .....

Indian Institute of Technology Delhi

HAUZ KHAS, NEW DELHI- 110016

Department/Centre/School of .....

Continuing Education Programme

On

Title of the Programme

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Mr./Ms. **Name Of The Participant**

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Prof.
Programme Coordinator

Prof.
Head of the Department

Prof.
Head/Associate Head, QIP/CEP

An initiative under eVIDYA@IITD (ई-विद्या@IITD)

Participants who are unable to score 50% marks in the evaluation but maintain a minimum attendance of 50% will be eligible for the **'Participation Certificate'** from CEP, IIT Delhi.

- The above e-certificate is for illustrative purposes only and the format of the certificate may be changed at the discretion of IIT Delhi.
- Only e-certificate will be provided and it will be issued by CEP, IIT Delhi.
- The organizing department of this programme is the Centre for Applied Research in Electronics (CARE) at IIT Delhi.

PROGRAMME COORDINATOR

PROF. ANKUR GUPTA

Associate Professor,
Centre for Applied Research in Electronics, IIT Delhi

Dr. Ankur Gupta is an associate professor in the Centre for Applied Research in Electronics (CARE) at IIT Delhi. He is also a core member of the VLSI Design Tools and Technology (VDTT) programme offered jointly with the Electrical Engineering and Computer Science department. He holds a master's degree in VLSI & Embedded Systems and Ph.D. Degree in Micro-electronics. He has more than 12 years of experience in VLSI and Microelectronics. He also has more than 6 years of Industrial experience with world's top MNCs i.e. Intel Inc., Texas Instruments and Global Foundries.

ABOUT IIT DELHI

Ranked 2nd as per QS World University Ranking (2024) in India

Ranked 2nd as per NIRF India Engineering Rankings (2024)

The Indian Institute of Technology Delhi (IIT Delhi) is one of the 5 initial IITs established for training, research and development in science, engineering and technology in India. Established as College of Engineering in 1961, the Institute was later declared as an Institution of National Importance under the "Institutes of Technology (Amendment) Act, 1963" and was renamed as "Indian Institute of Technology Delhi". It was then accorded the status of a Deemed University with powers to decide its own academic policy, to conduct its own examinations, and to award its own degrees.

Since its inception, over 48000 students have graduated from IIT Delhi in various disciplines, including Engineering, Physical Sciences, Management, Humanities and Social Sciences. Of these, nearly 5070 received Ph.D. degrees. The rest obtained a Master's Degree in Engineering, Sciences and Business Administration. These alumni today work as scientists, technologists, business managers and entrepreneurs. There are several alumni who have moved away from their original disciplines and have taken to administrative services, active politics, or are with NGOs. In doing so, they have significantly contributed to the building of this nation and to industrialization around the world.

ABOUT CONTINUING EDUCATION PROGRAMME (CEP)

Executive education is a vital need for companies to build a culture that promotes newer technologies and solutions and builds a workforce that stays abreast of the rapidly transforming needs to the technological, business and regulatory landscape. Committed to the cause of making quality education accessible to all, IIT Delhi has launched Online Certificate Programmes under eVIDYA@IITD (ई-विद्या@IITD): enabling Virtual & Interactive-learning for Driving Youth Advancement@IITD for Indian as well as international participants. These outreach programmes offered by the Indian Institute of Technology Delhi (IIT Delhi) are designed to cater to the training and development needs of various organisations, industries, society and individual participants at national and international level with a vision to empower thousands of young learners by imparting high-quality Online Certificate Programmes in cutting-edge areas for their career advancement in different domains of engineering, technology, science, humanities and management.

jaro education

Connect With
Us Now!

Jaro's Programme Expert

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For any feedback, please write to CEP, IIT Delhi at
contactcep@admin.iitd.ac.in

Online Certificate Programmes are offered by the Indian Institute of Technology Delhi under the aegis of Continuing Education Programme (CEP) so that the Institute can realise its vision of serving as a valuable resource for industry and society, and fulfil its mission to develop human potential to its fullest extent so that intellectually capable and imaginatively gifted leaders can emerge in a range of professions.